IN THE SPECIFICATION

Please replace the paragraph beginning on page 4, line 14 with the following:

Most ISPs deliver the services described above using a network access server. These devices are a type of router that is specifically designed for the task of routing traffic between a large number of low-speed interfaces (called ingress interfaces) and a small number of high-speed interfaces (called egress interfaces). Such servers, like other routers, use a packet forwarding engine to process and route incoming packets to an appropriate outgoing interface. But in addition to packet forwarding, access servers perform a variety of other specialized, data processing-intensive tasks that are not typically found in other types of routers. These functions are, e.g., those required to support PSTN signaling and bearer channel formats, deliver dial-in PPP endpoint and modem functionality, private network tunneling endpoint functionality, and VoIP-to-PCM conversion. As a result, access servers typically use a high-speed forwarding engine for packet processing and routing, and multiple digital signal processors (DSPs) to provide ~~modemand~~ modem and voice packetization services on the ingress ports.

Please replace the paragraph beginning on page 12, line 23 with the following:

The backplane of chassis 100 comprises three primary buses—a backplane FE interconnect 102, a maintenance bus 104, and a TDM bus 106. Backplane FE interconnect 102 comprises twenty-four point-to-point, full-duplex 100 Mbps FE links. Each link connects one of slots ~~0-6~~ 0-5 and 8-13 to slots 6 and 7. Maintenance bus 104 is a controller area network bus, which uses a two-wire serial multi-master interface that provides a maximum transfer rate of 1 Mbps. TDM bus 106 is actually an aggregation of four separate circuit-switched buses, each supporting 2048 bi-directional 64 kbps channels. Each of the resulting 8192 channels is accessible at each of slots 0-5 and 8-13. Not shown is a reference clock line for the TDM bus—the source of the reference clock can be selected as either a front panel-connected reference on one of RSC0 and RSC1, an internally-generated free-running clock on one or RSC0 and RSC1, or a signal derived from any trunk port on one of the line cards. Also not shown is a bus linking RSC0 and RSC1 to backplane nonvolatile random-access memory (NVRAM), which stores MAC addresses for the chassis, etc.

Please replace the paragraph beginning on page 36, line 6 with the following:

An access server architecture, and methods for use of the architecture to increase the scalability of and balance processor load for a network access server device, are disclosed.

~~The architecture and methods are designed to increase the scalability of and balance processor load for a network access server device~~. In this architecture, packet forwarding and packet processing are distributed amongst ~~the~~ cards serving ~~the~~ low-speed access lines (i.e., line cards~~), such that each line card is responsible for performing forwarding and packet processing for packets associated with the low-speed ports that line card serves~~. Thus, as the number of line cards expands, forwarding resources are expanded in at least rough proportion. The NAS route switch controller~~, as well as~~ and the high-speed ports used to access the network~~,~~ are largely relieved of packet processing tasks for traffic passing through the server. The egress port uses a distribution engine that performs the routing lookup for packets received at the high-speed interface, tags the packets with an adjacency table pointer, and sends them to the appropriate forwarding engine for packet processing. The route switch controller, largely uninvolved in the processing of packets, updates ~~the~~ routing information needed by each distribution or forwarding engine~~, and is largely uninvolved in the processing of individual packets~~.